IN THE CLAIMS

1. (Currently amended) A method of manufacturing a semiconductor device, the method comprising ~~the steps of~~:

forming a gate insulating layer on a semiconductor substrate;

forming a silicon gate layer on said gate insulating layer;

forming gate lines by patterning said silicon gate layer;

performing an impurity implantation ~~by~~ on the semiconductor substrate, using said gate lines as a mask;

forming an etch stop layer overlying the resulting structure including the gate lines;

forming an interlayer insulating layer ~~over said substrate over which~~ on said etch stop layer ~~impurity implantation is carried out~~;

exposing a surface of said silicon gate layer of said gate lines through said etch stop layer ~~by planarizing said interlayer insulating layer~~; and

forming a metal silicide layer on ~~an~~ the exposed surface of said silicon gate layer.

2. (Currently amended) The method of manufacturing a semiconductor device according to claim 1,

further including ~~the steps of~~ forming openings to expose a ~~given~~ region of said substrate by partially etching said interlayer insulating layer after said ~~step of~~ forming said interlayer insulating layer, and filling said openings by depositing a silicon layer; and

wherein said ~~step of~~ exposing the surface of said silicon gate layer of said gate lines includes planarizing said silicon layer.

3. (Currently amended) The method of manufacturing a semiconductor device according to claim 1, wherein said ~~step of~~ forming said metal silicide layer comprises:

depositing a metal layer by a sputtering process;

annealing said metal layer; and

removing non-reacted residual metal by an etching process.

4. (Currently amended) A method of forming a cell area of a flash memory device comprising ~~the steps of~~:

forming an active region having a plurality of line shaped sub-regions on a semiconductor substrate, each being defined parallel to each other by an isolation layer;

PAGE 6/11 * RCVD AT 12/20/2004 1:23:46 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:5032744622 * DURATION (mm-ss):03-24

forming a gate insulating layer and a silicon floating gate layer in said active region;

forming a floating gate intermediate pattern by patterning said floating gate layer;

forming a dielectric layer over the whole surface of said substrate over which said floating gate intermediate pattern is formed;

forming a silicon control gate layer over said substrate over which said dielectric layer is formed;

forming a plurality of gate lines in a direction vertical to a direction forming said active region by etching partially said silicon control gate layer, said dielectric layer, and said floating gate intermediate pattern;

doping said active region between said gate lines by using a dose of impurity below 1.0×10^{15} ions/ cm^2;

forming a lower interlayer insulating layer over the whole surface of said substrate over which said doping is carried out;

forming a groove exposing a common source region in said active region by etching partially said lower interlayer insulating layer;

depositing a silicon layer to fill said groove;

forming a wall shaped silicon common source line with exposing upper portions of said gate lines by planarizing said silicon layer and said lower interlayer insulating layer; and

forming a metal silicide layer on exposed upper surfaces of said gate lines and on said silicon common source line.

5. (Currently amended) The method of forming a cell area of a flash memory device according to claim 4, further including ~~the step of~~ forming an etch stop layer over ~~the whole surface of~~ said substrate between said ~~step of~~ doping and said ~~step of~~ forming said lower interlayer insulating layer.

6. (Currently amended) The method of forming a cell area of a flash memory device according to claim 4,

wherein said ~~step of~~ forming said groove includes forming contact holes in bit line contact regions; and

further including ~~the steps of~~:

forming an upper interlayer insulating layer after said ~~step of~~ forming said metal silicide layer;

PAGE 7/11 * RCVD AT 12/20/2004 1:23:46 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:5032744622 * DURATION (mm-ss):03-24

forming contact holes in said bit line regions by etching partially said upper interlayer insulating layer;

depositing a wiring metal layer for bit lines and bit line contacts; and

forming bit lines by patterning said wiring metal layer.

7. (New) The method of manufacturing a semiconductor device according to claim 2, further comprising forming a silicide layer on said planarized silicon layer.

8. (New) A method of forming a semiconductor device comprising:

forming an active region on a semiconductor substrate, the active region defined by an isolation layer;

sequentially forming a gate insulating layer and a silicon floating gate layer on the active region;

forming a floating gate intermediate pattern by patterning the floating gate layer;

forming an intergate dielectric layer overlying the floating gate intermediate pattern;

forming a silicon control gate layer overlying the intergate dielectric layer;

forming a plurality of gate lines by sequentially patterning the silicon control gate layer, the dielectric layer, and the floating gate intermediate pattern;

forming a lower interlayer insulating layer overlying the plurality of gate lines;

forming a groove to expose a common source region in the active region by etching a portion of the lower interlayer insulating layer;

depositing a silicon layer to fill the groove;

forming a silicon common source line and exposing upper portions of the gate lines by planarizing the silicon layer and the lower interlayer insulating layer; and

forming a metal silicide layer on exposed upper surfaces of the gate lines and on the silicon common source line.

9. (New) The method of claim 8, further comprising forming an etch stop layer over the gate lines before forming the lower interlayer insulating layer.

PAGE 8/11 * RCVD AT 12/20/2004 1:23:46 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:5032744622 * DURATION (mm-ss):03-24